Neutron induced single event effects on integrated circuits: testing results and mitigation strategies

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Reliability and Radiation Effects on Advanced CMOS Technologies
Introduction

Neutron induced SEEs scaling with Moore’s law

SRAM data as benchmark

Neutron effects on Flash memories (Floating gate)

Summary
Industrial sectors

• **Aerospace**
  – Satellites
  – Civilian and military aircraft

• **Medical**
  – Implanted electronic devices (pacemakers, defibrillators…)

• **Nuclear Industry**
  – Instrumentation and control in proximity to reactors

• **Transport**
  – Electronics in cars and trains
  – Signalling and traffic control networks

• **IT Networks and Telecommunication**…
We have performed several neutron test shifts at ISIS-RAL labs (Dr. C. Frost), UK, in collaboration with CNR, Univ. Roma-Tor Vergata (prof. Andreani, prof. Salsano) and Univ. Milano Bicocca (prof. Gorini) groups; we have also tested several samples at TRIUMF (Vancouver, Can) and LANSCE (Los Alamos, NM, USA)
Neutrons are the biggest concern today, but muons are even more abundant at sea level.

 Thermal neutrons are ubiquitous.
Stochastic (i.e., unpredictable) effects, resulting in malfunctioning of an electronic device/circuit/system, due to a single particle hitting a sensitive area (→ SEE cross section, cm$^2$) of a chip at the wrong time

- **Non-destructive**
  - Single Event Upsets (SEU) → Soft Error → **Soft Error Rate (SER)**
  - Single Bit Upsets (SBU)
  - Multiple Cell Upsets (MCU)
  - Multiple Bit Upsets (MBU)
  - Single Event Transients (SET)
  - Single Event Functional Interrupts (SEFI)

- **Destructive**
  - Single Event Gate Rupture (SEGR)
  - Single Event Burnout (SEB)

- **Possibly Destructive**
  - Single Event Latch-up (SEL)
  - Single Event Snapback (SES)
Moore’s law is (self-)validated by reducing the device dimension over the years, by scaling down the **minimum feature size** of the CMOS technology node.

**Source:** INTEL
Simulated heavy ion e-h track in Si

Fe ions 275 MeV
LET=24 MeV cm²/kg

LET metrics in Si:
1 MeV cm²/kg
6.4\times10^4 e-h pairs/µm
10 fC/µm

Electron-Hole density (cm⁻³)

P. Fouliiat, EWRHE 2004
Heavy ion e-h track in Si vs. CMOS minimum size

CMOS generation

- 0.35 µm
- 0.25 µm
- 0.18 µm
- 0.13 µm
- 90 nm
- 32 nm

DEDHIS Fer 275Me
SRAM n-induced SEU scaling trends (2005)

R. Baumann, IEEE-TDMR, 2005

A. Paccagnella – ASI, 8/6/2015
SRAM n-induced SEU scaling trends (2013)

- Per bit, SER has peaked at 130 nm and then has been decreasing with each CMOS generation.
- However, due to the increase of the bit number, the system sensitivity has kept increasing.
- MBU have increased as well.

Courtesy: Robert Baumann, 2013
Multiple Bit Upsets induced by neutrons

Percentage of **Multiple Bit Upsets** increases in CMOS, more difficult to correct by ECC

*N. Seifert, et al., IRPS 2008*
**Flash memories: neutron effects**

- **NAND Flash** memories (using Floating Gate MOSFETs, FG): the most advanced microelectronic technologies and feature the **smallest minimum feature size: 16 nm**
- There is **no rad-hard alternative** to these chips (COTS)
- Until a **few years ago:**
  - Only effects in the peripheral circuitry were of concern
  - Charge pumps weakest component
- In 2008 we demonstrated (*G. Cellere, et al., 2008 IEEE-IEDM*) that **atmospheric neutrons may produce upsets** in commercial Flash components
- **Nowadays:**
  - Effects in the peripheral circuitry are still very important but **FG array sensitivity** is an issue as well, as they may occur even on idle/off devices
When the threshold voltage shift is large enough to bring the cell beyond the read voltage, an error occurs.

Intermittent errors may take place when $V_{th}$ close to read voltage.

A. Paccagnella – ASI, 8/6/2015
Neutron induced $V_{th}$ tails

S. Gerardin, et al. TNS, 2010

- 2-bit-per-cell memory: 4 $V_{th}$ levels are needed
- Atmospheric-like neutrons produce:
  - Secondary charged byproducts, which in turn produce…
  - Linear $V_{th}$ tails in log-lin scale

65-nm NOR Flash memories irradiated with $3.6 \cdot 10^{10}$ cm$^{-2}$ neutrons with atmospheric-like spectrum
In addition to the large energy depositions caused by ions going through FG (large events)...

greater are several small depositions by energetic electrons going through FG (small events, GEANT4 simulations): we can think of them in terms of total dose.

S. Gerardin, et al. TNS, 2010
Geant4 used to assess neutron byproducts, heavy-ion and x-ray data for conversion coefficients.

Small events fit the tail at lower $V_{th}$.

Large events fit the tail at higher $V_{th}$.

Good agreement despite limitations (energies, angles of heavy ions used for conversion).

Tail on L3 for 65-nm NOR Flash memories irradiated with $3.6 \times 10^{10}$ cm$^{-2}$ neutrons with atmospheric-like spectrum.
Neutron FG error cross section

MLC samples

![Graph showing Bit σ vs Node [nm] for MLC samples.

SLC samples

![Graph showing Bit σ vs Node [nm] for SLC samples.

S. Gerardin, et al., TNS 2014

- σ exponentially increases as the cell feature size is reduced
- The FG error bit σ for 25-nm is >10x than for 50-nm NAND
- 34-nm SLC: first SLC generations sensitive to neutrons
- The neutron cross section of 34-nm SLC is more than 3 orders of magnitude smaller with respect to 25-nm MLC samples
- The neutron cross section is obtained and fitted to our experimental data
- A turnaround is expected between 10 and 20 nm
  - For one or few more generations we expect the neutron $\sigma$ to increase
  - Afterwards a significant decrease should occur, due to the fact that the FG becomes smaller and smaller than the heavy-ion track

*S. Gerardin, et al., TNS 2014*
Neutron effects on electronics are an important concern for many industries and applications.

The SRAMs benchmark shows a per-bit SER reduction at minimum feature size <180nm, but the system SER increases due the ever-increasing bit density per chip.

Flash memories are produced in the most advanced CMOS technology nodes and are sensitive to neutron induced SEE.

At sea level, the soft error rates of Flash memories can be covered by current specified ECC.

In more aggressive radiation environments, proper mitigation techniques must be adopted, to ensure correct operations (see next talk by prof. G.C. Cardarilli!)